(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number : **0 603 106 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number : **93480199.4**

(51) Int. Cl.^{5} : **H01L 21/76**

(22) Date of filing : **19.11.93**

(30) Priority : **16.12.92 US 991010**

(43) Date of publication of application :
22.06.94 Bulletin 94/25

(84) Designated Contracting States :
DE FR GB

(71) Applicant : **International Business Machines Corporation**
Old Orchard Road
Armonk, N.Y. 10504 (US)

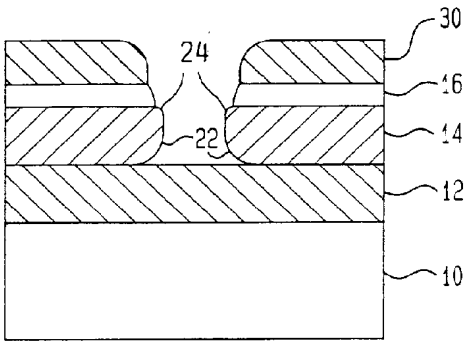
(72) Inventor : **Chidambarrao,Dureseti**
5 Clearview Drive
Sandy Hook,Connecticut 06482 (US)
Inventor : **Hsu, Louis Lu-Chen**
7 Crosby Court
Fishkill, NY 12524 (US)
Inventor : **Mis, Daniel J.**
24 Horizon Hill Drive
Poughkeepsie, NY 12603 (US)
Inventor : **Peng, James Ping**
20 Kellerhause Drive
Poughkeepsie, NY 12603 (US)

(74) Representative : **Klein, Daniel Jacques Henri**
Compagnie IBM France
Département de Propriété Intellectuelle
F-06610 La Gaude (FR)

(54) Method to reduce stress from trench structure on SOI wafer.

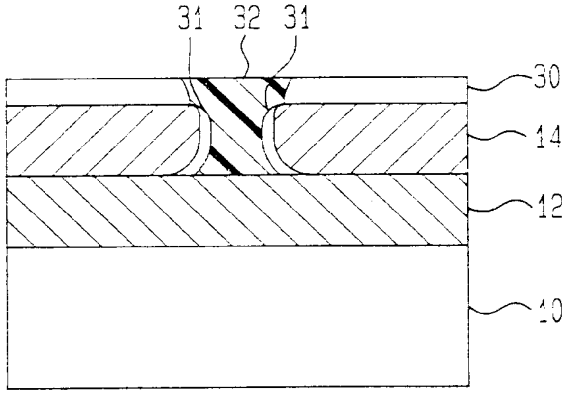
(57) In an isolation trench in a silicon-on-insulator wafer, the sidewalls of the trench curve outwardly at the bottom of the trench where the top silicon layer meets the underlying oxide insulating layer. A typical SOI structure is comprised of a semiconductor substrate (10), a silicon-oxide (SiO_2) layer 12, and a single crystal silicon layer (14). A suitable masking oxide layer (16) is deposited on the top surface of the silicon layer (14) and a photoresist (30) is formed thereon. The photoresist (30) is developed in the desired trench pattern and an opening for the trench is formed in the oxide mask (16) by means of well-known semiconductor process steps. An isolation trench (20) is formed in the top single crystal silicon layer (14) so that its sidewalls (22), at the bottom of the trench curve outwardly from the center of the trench. Preferably, the top corners (24) of the trench sidewalls are also slightly rounded to further reduce points of stress. After the trench is formed, the photoresist is removed and an oxide layer (31) is grown on the trench sidewalls using a conventional process. The trench is then filled with polysilicon (32) using a conventional chemical vapor deposition process. Finally, the structure is planarized. Optionally a stress relief annealing step is carried out at about 1050°C to 1100°C for about 20 minutes in a forming gas. This sidewall geometry eliminates the sharp corner at the bottom of the trench that are detrimental to device reliability.

FIG. 1E



EP 0 603 106 A2

FIG. 1G



The present invention generally relates to an improved isolation trench geometry for trenches formed in silicon-on-oxide wafers, and more particularly to a geometry that reduces structural stress in the trench wall, and includes a process for forming such isolation trenches.

Building semiconductor devices on silicon-on-insulator (SOI) wafers is recent technology that has been introduced to improve circuit speed and device reliability. Depending on the circuit application, the thickness of the top silicon layer of a silicon-on-insulator wafer will vary from 0.05 μm to 15 μm. Normally, SOI device applications can be divided into three categories: (a) high density, low power digital CMOS applications where a thin silicon layer (about 0.05 to 0.2 μm) is desirable to form fully depleted MOS devices; (b) medium density, high speed and low voltage digital BiCMOS applications where a silicon thickness of 1.5 to 3.0 μm is needed in order to achieve optimum bipolar performance, i.e., high cut-off frequency; and (c) low density, high speed and high voltage analog BiCMOS devices where a large silicon thickness ranging from 8 to 15 μm is necessary in order to withstand high voltage operation.

Since each of these three SOI devices requires a different range of silicon layer thickness and different integrated device density, quite different isolation schemes are needed. For case (a) with the thin SOI, the isolation is usually formed by using a conventional recess oxidation (ROX) process. For Case (b) with the medium thickness SOI, trench isolation with an oxide sidewall and polysilicon fill is used. Lastly in case (c) with the thick SOI where there is a power limitation which allows only low density integration, simple junction isolation is adequate.

In cases (a) and (b), the prior art isolation recess or trench can develop regions of large stress. Ion implantation in these stress regions can result in a nucleate glide dislocation that can cause shorts or leakage in transistors.

An object of this invention is the provision of a silicon-on-insulator isolation trench free of geometrics that result in high stress in the silicon trench wall.

Another object of this invention is the provision of a method of forming a silicon-on-insulator isolation trench so that the trench sidewall is free of high stress producing sidewall geometries.

Briefly, this invention contemplates the provision of an isolation trench in a silicon-on-insulator wafer in which the sidewalls of the trench curve outwardly at the bottom of the trench where the top silicon layer meets the underlying oxide insulating layer. This sidewall geometry eliminates the sharp corner at the bottom of the trench. Preferably, the top edge of the trench wall is also curved.

To form the trench with an outwardly curving wall surface at the bottom of the trench, a trench etch is used that has a highly selective etch rate of silicon as compared to oxide. For example, an SF_6/Cl_2 plasma etches silicon at a rate that is 12 times faster than it etches silicon oxide. When the oxide layer of the silicon-on-insulator wafer is reached and exposed to such an etch, the vertical etch rate is significantly reduced. Over etching the trench into the oxide layer results primarily in a lateral undercutting at the bottom of the silicon trench walls. Any one of several methods can be used to determine when the top surface of the sub-oxide layer is reached; optical emission, a laser interferometer, or the etch can be timed. The degree of outward curvature can be controlled by controlling the duration of the over etch after the sub-oxide layer is reached. In a preferred embodiment, the top edge of the trench is rounded by ion sputtering during a final stage of the trench formation.

The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of a preferred embodiment of the invention with reference to the drawings, in which:

Figures 1A through 1G illustrate a trench structure in accordance with the teachings of this invention at successive stages in its fabrication; Figure 1E shows the completed trench structure with the sidewall of the trench curved outwardly at the bottom of the trench.

Referring now to Figure 1A, it shows a fragmentary, sectional view of a conventional silicon-on-insulator wafer for a medium density, high speed, low voltage digital BiCMOS applications. The wafer is comprised of a semiconductor substrate 10, a silicon-oxide (SiO_2) layer 12, and a single crystal silicon layer 14 whose thickness is on the order of between 1.5 μm and 3.0 μm. A suitable masking oxide layer 16 is deposited on the top surface of the silicon layer 14 and a photoresist layer 30 is formed in the oxide mask layer 16. The photoresist 30 is developed in the desired trench pattern and an opening for the trench is formed in the oxide mask 16 by means of well-known semiconductor process steps.

Referring now to Figure 1B, an isolation trench 20 is formed in the top single crystal silicon layer 14 so that its sidewalls 22, at the bottom of the trench curve outwardly from the center of the trench. The radius of outward curvature R should be in a range between that of the sidewall oxide thickness (between 50 nm and 100 nm) and 25% of the thickness of the silicon layer 14.

To form the trench 20 with sidewalls 22 that curve outwardly from the bottom, an etching process is used that etches the silicon layer 14 selectively at a much higher rate than it etches the silicon-oxide layer 12. For example, a conventional SF_6/Cl_2 plasma etching process is suitable as it has a selectivity ratio of 12 to 1; that is, a SF_6/Cl_2 plasma etches the silicon layer 14 at twelve times the rate it etches the silicon-oxide layer 12. Other suitable known etching processes are Cl_2/O_2 plasma which has a similar selectivity.

When the etching process has proceeded to the point where the surface of the oxide layer 12 is exposed, the rate of vertical etching is greatly reduced. Continued etching beyond this point results in a lateral undercutting of the silicon layer 14 at the bottom of the trench as shown in Figure 1B. The duration during which the etch process continues after the oxide layer is exposed, determines the radius of curvature R of the outwardly sloping sidewalls; the radius increases as the duration increases.

The top surface of the sublayer oxide 12 can be detected by a suitable method such as optical emission, laser interferometer or timing the etch. Typically, by monitoring Cl emission line (wavelength 308 nm) a reproducible end point characteristic can be obtained. Normally several large end point test sites are located on the wafer. The degree of convexness of the silicon bottom can be controlled by controlling the percentage of overetch.

Preferably, the top corners 24 of the trench sidewalls are also slightly rounded to further reduce points of stress. To this end, the photoresist layer 30 is pulled back slightly from the trench opening by means, for example, of an O 2 plasma etch that exposes a small region 23 of the surface of the oxide layer 16, as shown in Figure 1C. Next, the exposed surface of the oxide layer 16 is trimmed away by means of a CF_4 plasma etch step to expose the top corners of the trench in silicon layer 14. The structure at this stage is shown in Figure 1D. A Cl_2O_2 plasma etch for a brief interval is used to cut away and thereby round the top corners 24 of the trench sidewall as shown in Figure 1E.

After the trench is formed, the photoresist is removed, an oxide layer 31 is grown on the trench sidewalls using a suitable prior art process such as conventional thermal oxidation at 950°C or high pressure oxidation at 700°C to grow oxide about 60 nm thick as shown in igure 1F. The trench is then filled with polysilicon 32 using a conventional chemical vapor deposition process. After planarization, the structure at this stage is shown in Figure 1G. After the structure is completed to this stage, a stress relief annealing step is preferably carried out at about 1050°G to 1100°C for about 20 minutes in a forming gas (e.g. 10% H_2, 90°N_2).

Claims

1. In a silicon-on-insulator wafer comprised of a silicon layer on an insulating layer, an isolation trench formed by an opening in said silicon layer that extends from a top surface of said silicon layer to a top surface of said insulating layer, said opening formed by vertical sidewalls that each has a curved surface that curves away from a vertical center line of said opening where said sidewalls meet said top surface of said insulating layer.

2. In a silicon-on-insulator wafer comprised of a silicon layer on an insulating layer, an isolation trench as in claim 1, wherein said curve has a radius of curvature in a range extending at the low end between 500Å and 1000Å to 25% of the thickness of said silicon layer.

3. In a silicon-on-insulator wafer comprised of a silicon layer on an insulating layer, an isolation trench as in claim 1, wherein each of said vertical sidewalls is curved at said top surface of said silicon layer.

4. In a silicon-on-insulator wafer comprised of a silicon layer on an insulating layer, an isolation trench as in claim 2, wherein each of said vertical sidewalls is curved at said top surface of said silicon layer.

5. A method of forming an isolation trench in a silicon-on-insulator wafer including a silicon layer overlying an insulator layer, comprising the steps of:

etching through said silicon layer to said insulator layer with an etchant that selectively etches said silicon layer at a high rate compared with the rate at which it etches said insulator layer;

continuing the etching process of said previous step for a predetermined interval so that walls formed in said layer are undercut where they meet said insulator layer.

6. A method of forming an isolation trench in a silicon-on-insulator wafer including a silicon layer overlying an insulator layer, comprising the steps of:

etching a trench opening into said silicon layer through a masking layer that overlies said silicon layer, said trench opening forming a top edge at the upper surface of said silicon layer;

removing a small portion of said masking layer to expose a region of said silicon layer extending away from the top edges of said trench opening formed in the previous step;

etching said region of said silicon layer to form a curve at said top edges of said trench opening.

7. A method of forming an isolation trench in a silicon-on-insulator wafer including a silicon layer overlying an insulator layer, comprising the steps of:

etching through a masking layer that overlies said silicon layer to said insulator layer with

an etchant that selectively etches said silicon layer at a high rate compared with the rate at which it etches said insulator layer;

continuing the etching process of said previous step for a predetermined interval so that walls formed in said layer are undercut where they meet said insulator layer with said trench opening forming a top edge at the upper surface of said silicon layer;

removing a small portion of said masking layer to expose a region of said silicon layer extending away from the top edges of said trench opening formed in the previous step;

etching said region of said silicon layer to form a curve at said top edges of said trench opening.

8. A method of forming an isolation trench in a silicon-on-insulator wafer including a silicon layer overlying an insulator layer as in claim 6, including the further steps of annealing said silicon-on-insulator wafer in a forming atmosphere.

9. A method of forming an isolation trench in a silicon-on-insulator wafer including a silicon layer overlying an insulator layer as in claim 7, including the further steps of annealing said silicon-on-insulator wafer in a forming atmosphere.

FIG. 1A

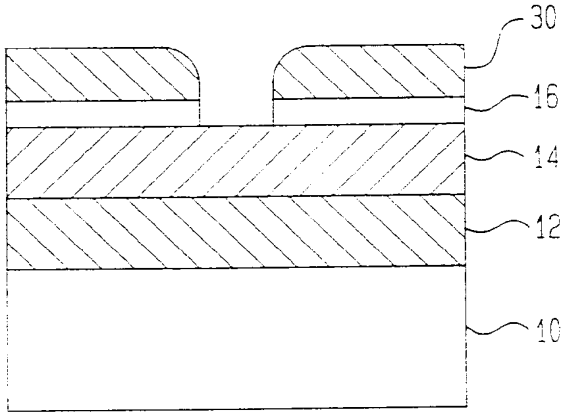


FIG. 1B

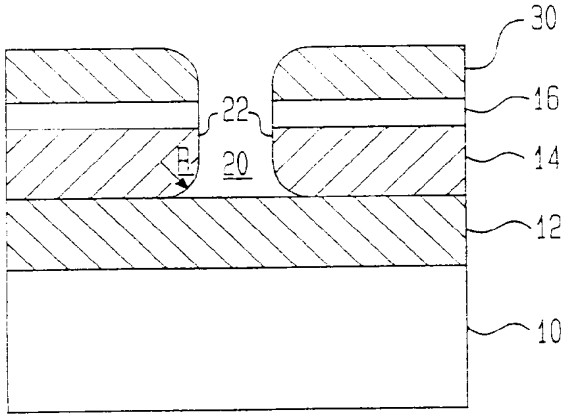


FIG. 1C

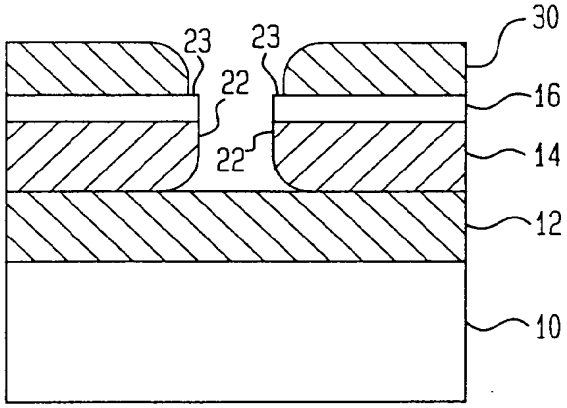


FIG. 1D

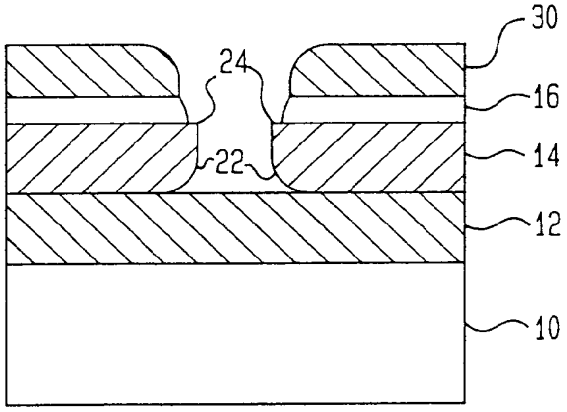


FIG. 1E

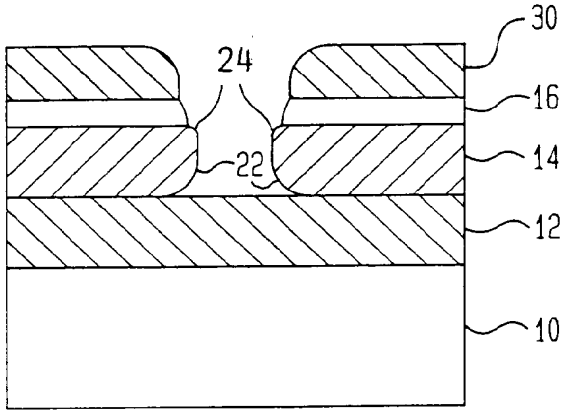


FIG. 1F

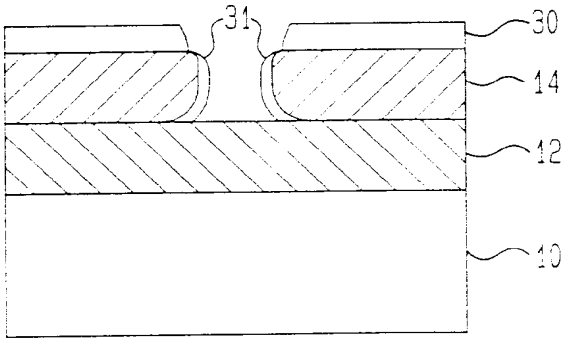


FIG. 1G